

# EMM 2114

## SEMI 2114 STATIC, TTL IN/OUT 1024x4 N-MOS RAM's

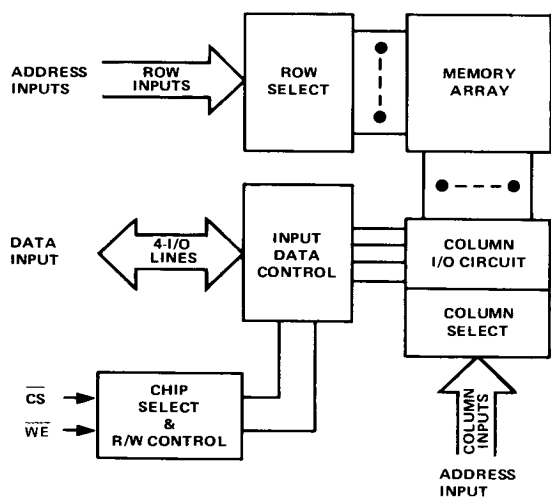
### FEATURES

- 1024 words x 4 bits
- Three access times (200, 300, and 450 nsec)
- Low operating power — 175 mW typical
- Standard power — 222 mW typical
- Common output bus
- Common output bus
- Three-state output drivers
- Fully STATIC — no clock or refresh
- Single +5V power supply
- TTL compatible interface
- 18-pin ceramic, plastic or cerdip package

### GENERAL DESCRIPTION

SEMI's Series 2114 RAMs are 1024 word x 4 bit static N-MOS Random Access Memories. These fully static memory cells require no external clocks, strobes or data refresh circuitry. TTL compatible THREE-STATE output drivers allow the use of common I/O lines—ideally suited for microprocessor interfacing to a common I/O bus. A single +5V input is the only power supply requirement. Read/ Write functions are controlled by the low state of  $\overline{\text{CS}}$  and the concurrent *high* or *low* level of Write Enable ( $\overline{\text{WE}}$ ) to initiate a Read or Write cycle respectively— with no pulse or edge triggering required. With  $\overline{\text{CS}}$  high (STANDBY), a high impedance is reflected to the I/O bus—resulting in a no-load condition when non-selected. The 2114 is available in a choice of access times, power dissipation and packaging to meet your particular requirement.

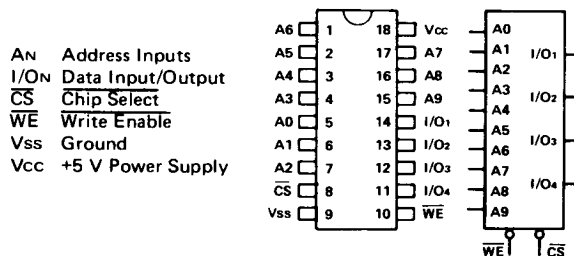
### BLOCK DIAGRAM



### TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{WE}}$	DI/DO	STATUS	MODE
H	Don't Care	High Z	Deselect	Standby
L	H	Data	Selected	Read
L	L	L	Selected	Write 0
L	L	H	Selected	Write 1

### PIN CONFIGURATION AND LOGIC SYMBOL



**EMM SEMI 2114 STATIC, TTL IN/OUT 1024x4 N-MOS RAM's**

**RECOMMENDED OPERATING CONDITIONS (T<sub>AMB</sub> = 0°C to 70°C)**

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V
Input High Level	V <sub>IH</sub>	2.0	—	5.25	V
Input Low Level	V <sub>IL</sub>	-0.5	—	0.8	V

**DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range)**

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I <sub>LI</sub>	-10	—	+10	μA	V <sub>IN</sub> = 0 to 5.25V
I/O Leakage Current	I <sub>LO</sub>	-10	—	+10	μA	V <sub>I/O</sub> = 0.4 to 5.25V, CS = 2.4V
Output Voltage High	V <sub>OH</sub>	2.4	—	—	V	I <sub>O</sub> = -1.0ma
Output Voltage Low	V <sub>OL</sub>	—	—	0.4	V	I <sub>O</sub> = 2.1 ma
Power Supply Current						
2114-2,3	I <sub>CC</sub>	—	50	70	ma	T <sub>AMB</sub> = 25°C
	I <sub>CC</sub>	—	—	100	ma	T <sub>AMB</sub> = 0°C to 70°C
L2114-2,3	I <sub>CC</sub>	—	35	65	ma	T <sub>AMB</sub> = 25°C
	I <sub>CC</sub>	—	—	70	ma	T <sub>AMB</sub> = 0°C to 70°C
2114-U	I <sub>CC</sub>	—	45	75	ma	T <sub>AMB</sub> = 25°C
	I <sub>CC</sub>	—	65	100	ma	T <sub>AMB</sub> = 0°C to 70°C
L2114-U	I <sub>CC</sub>	—	35	45	ma	T <sub>AMB</sub> = 25°C
	I <sub>CC</sub>	—	40	70	ma	T <sub>AMB</sub> = 0°C to 70°C

**READ CYCLE — AC CHARACTERISTICS (CONDITIONS—Full Operating Voltage and Temperature Range)**

PARAMETER	SYMBOL	2114-2, L2114-2			2114-3, L2114-3			2114-U, L2114-U			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	T <sub>RC</sub>	200	—	∞	300	—	∞	450	—	∞	ns
Access Time	T <sub>A</sub>	—	—	200	—	—	300	—	—	450	ns
Chip Select-to-Output, Valid	T <sub>CO</sub>	—	—	70	—	—	100	—	—	120	ns
Chip Select-to-Output, Active	T <sub>CX</sub>	20	—	—	20	—	—	20	—	—	ns
Output Hold After Address Change	T <sub>OHA</sub>	50	—	—	50	—	—	50	—	—	ns
Output Disable After Chip Deselection	T <sub>OTD</sub>	—	—	60	—	—	80	—	—	100	ns

**WRITE CYCLE — AC CHARACTERISTICS (CONDITIONS—Full Operating Voltage and Temperature Range)**

PARAMETER	SYMBOL	2114-2, L2114-2			2114-3, L2114-3			2114-U, L2114-U			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	T <sub>WC</sub>	200	—	∞	300	—	∞	450	—	∞	ns
Write Pulse Width	T <sub>W</sub>	120	—	—	150	—	—	200	—	—	ns
Write Recovery Time	T <sub>WR</sub>	0	—	—	0	—	—	0	—	—	ns
Data Setup Time	T <sub>DW</sub>	120	—	—	150	—	—	200	—	—	ns
Data Hold Time	T <sub>DH</sub>	0	—	—	0	—	—	0	—	—	ns
Output Disable From Write or Chip Enable Time	T <sub>OTW</sub>	—	—	60	—	—	80	—	—	100	ns

**CAPACITANCE**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance	C <sub>IN</sub>	—	4	5	pF	V <sub>IN</sub> = 0V
Output Capacitance	C <sub>I/O</sub>	—	4	5	pF	V <sub>I/O</sub> = 0V



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**ABSOLUTE MAXIMUM RATINGS**  
(See Note 1) (Referenced to GND)

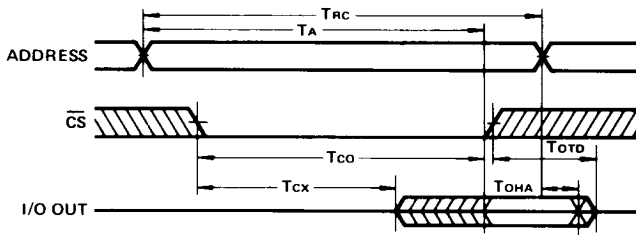
RATING	VALUE	UNIT
Voltage on Any Pin With Respect to GND	-0.5 to +7.0	Vdc
Power Dissipation	1.0 (NOTE 2)	W
Operating Ambient Temperature Range (T <sub>AMB</sub> )	0 to +70	°C
Temperature Under Bias (T <sub>BIAS</sub> )	-10 to +80	°C
Storage Temperature (T <sub>STOR</sub> )	-65 to +150	°C
Current Into/From Output (I <sub>O</sub> )	50	ma

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C Ambient. Derate 13.5 mw/°C.

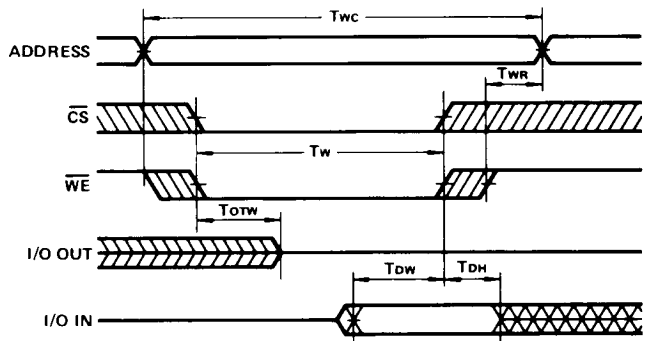
**READ CYCLE TIMING**



NOTES:

1. WE is high for a Read Cycle.
2. T<sub>w</sub> is measured from the latter of CS or WE going low to the earlier of CS or WE going high.
3. WE or CS must be high prior to a write cycle to prevent an erroneous write during the address transitions.

**WRITE CYCLE TIMING**



**FUNCTIONAL DESCRIPTION**

EMM SEMI's 2114 is a 4096 bit static RAM, organized in a 1024 word by 4 bit configuration. Each word is selectively accessed by address lines A<sub>0</sub> through A<sub>9</sub>, with data being read or written on common data input/output lines (I/O<sub>1</sub> through I/O<sub>4</sub>), as controlled by the Chip Select (CS) and Write Enable (WE) functions.

Since no address setup time is required, data access is quite simple. With WE high and CS low, the array may be read by simply toggling the input address. Valid data output becomes available after time T<sub>A</sub>, following each address change. However, should CS be used to control the read mode, valid data access time must be equal to or greater than T<sub>A</sub>, but cannot occur earlier than T<sub>CO</sub> from CS going low.

The write mode is enabled whenever CS and WE are both low. Stored data integrity is therefore preserved as long as either CS or WE is high. To write valid

data, the address input may be applied simultaneously with the write enable (CS and WE both low), but must remain stable for the period T<sub>wc</sub> while writing.

Possible write modes are as follows:

1. CS is held low. T<sub>w</sub> is then defined by WE going from a high state to a low state and T<sub>wr</sub> is defined by WE going from a low state to a high state.
2. WE is held low. CS going low is then used to define T<sub>w</sub>. CS going high is used to define T<sub>wr</sub>.
3. CS and WE are both used. T<sub>w</sub> timing is defined by the latter of CS or WE going low, and T<sub>wr</sub> timing is determined by the earlier of CS or WE going high.

The address must remain stable for the full Write cycle. However, data inputs are not required to remain stable for the full cycle. The correct logic level will be entered as long as input data is stable for the time period T<sub>ow</sub> during the write cycle.



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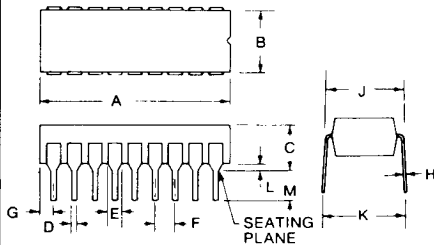
## FUNCTIONAL NOTES:

1.  $T_{AW}$  is measured from the latter of  $\overline{CS}$  or  $\overline{WE}$  going low.
2.  $T_w$  is measured from the latter of  $\overline{CS}$  or  $\overline{WE}$  going low, to the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high.
3.  $T_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high.
4.  $T_{DH}$  and  $T_{OW}$  are measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high.
5.  $T_{OTW}$  is measured from  $\overline{WE}$  going low or  $\overline{CS}$  going high, whichever occurs first.
6. Timing diagrams are based on loading to simulate the capacitive effect of twenty (20) additional outputs connected in parallel (100 pf) plus the current loading affect of one TTL input load.
7. Input pulse levels are 0.8 volts for logic low, to 2.0 volts for logic high.
8. Input rise and fall times are of equal value (10 ns).
9. Timing is measured from the 1.5 volt level whether the level is going high or low.
10. Each I/O line is a high impedance during the write mode, or when  $\overline{CS}$  is high. Inputs always represent a high impedance.

## ORDERING INFORMATION

DEVICE	ACCESS TIME	MAXIMUM POWER DISSIPATION	PACKAGE	TEMP. RANGE
2114-2CA	200ns	525mw	18-pin Ceramic	0° C to 70° C
2114-2CB	200ns	525mw	18-pin Plastic	0° C to 70° C
2114-2CE	200ns	525mw	18-pin Cerdip	0° C to 70° C
L2114-2CA	200ns	368mw	18-pin Ceramic	0° C to 70° C
L2114-2CB	200ns	368mw	18-pin Plastic	0° C to 70° C
L2114-2CE	200ns	368mw	18-pin Cerdip	0° C to 70° C
2114-3CA	300ns	525mw	18-pin Ceramic	0° C to 70° C
2114-3CB	300ns	525mw	18-pin Plastic	0° C to 70° C
2114-3CE	300ns	525mw	18-pin Cerdip	0° C to 70° C
L2114-3CA	300ns	368mw	18-pin Ceramic	0° C to 70° C
L2114-3CB	300ns	368mw	18-pin Plastic	0° C to 70° C
L2114-3CE	300ns	368mw	18-pin Cerdip	0° C to 70° C
2114-UCA	450ns	525mw	18-pin Ceramic	0° C to 70° C
2114-UCB	450ns	525mw	18-pin Plastic	0° C to 70° C
2114-UCE	450ns	525mw	18-pin Cerdip	0° C to 70° C
L2114-UCA	450ns	315mw	18-pin Ceramic	0° C to 70° C
L2114-UCB	450ns	315mw	18-pin Plastic	0° C to 70° C
L2114-UCE	450ns	315mw	18-pin Cerdip	0° C to 70° C

## TYPICAL OUTLINE DRAWING



## PACKAGING DIMENSIONS

DIM.	"B" PLASTIC PACKAGE				"A" CERAMIC PACKAGE				"E" CERDIP PACKAGE			
	MILLIMETERS		INCHES		MILLIMETERS		INCHES		MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	21.590	23.622	0.850	0.930	22.606	23.114	0.890	0.910	22.402	23.495	0.882	0.925
B	6.096	7.493	0.240	0.295	7.061	7.569	0.278	0.298	—	7.874	—	0.310
C	—	5.588	—	0.210	—	4.826	—	0.190	—	4.826	—	0.190
D	0.381	0.584	0.015	0.023	0.381	0.584	0.015	0.023	0.381	0.584	0.015	0.023
E	1.143	1.778	0.045	0.070	1.016	1.778	0.040	0.070	1.143	1.651	0.045	0.065
F	2.286	2.794	0.090	0.110	2.286	2.794	0.090	0.110	2.286	2.794	0.090	0.110
G	0.635	2.159	0.025	0.085	0.762	1.778	0.030	0.070	0.381	1.270	0.015	0.050
H	0.203	0.305	0.008	0.012	0.203	0.305	0.008	0.012	0.203	0.305	0.008	0.012
J	7.366	8.255	0.290	0.325	7.620	8.077	0.300	0.318	7.366	8.128	0.290	0.320
K	7.366	10.414	0.290	0.410	7.620 REF.	—	0.300 REF.	—	8.255	9.906	0.325	0.390
L	0.508	1.278	0.020	0.050	0.635	1.651	0.025	0.065	0.381	1.016	0.015	0.040
M	2.540	4.191	0.100	0.165	2.540	3.810	0.100	0.150	2.540	3.937	0.100	0.155

### WARNING:

#### MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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EMM SEMI reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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